HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 10981801-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Thomas J. Sullivan	**Confirmation No.:**	9074
Application No.:	09/491,810	**Examiner:**	Meonske, Tonia L.
Filing Date:	01/28/2000	**Group Art Unit:**	2183

Title: AN APPARATUS AND METHOD FOR PERFORMING SINGLE-INSTRUCTION MULTIPLE DATA INSTRUCTIONS

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **June 2, 2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: **July 19, 2005**

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number_____ on _____

Number of pages:

Typed Name: **Shana L. East**

Signature: Shana L. East

Respectfully submitted,

Thomas J. Sullivan

By _____

Jon E. Holland

Attorney/Agent for Applicant(s)
Reg. No. **41,077**

Date: **7/19/2005**

Telephone No.: **(256) 704-3900**

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: **Thomas J. Sullivan**			
Serial No.:	09/491,810	Art Unit:	2183
Filed:	January 28, 2000	Examiner:	Meonske. Tonia L.
For:	AN APPARATUS AND METHOD FOR PERFORMING SINGLE-INSTRUCTION MULTIPLE DATA INSTRUCTIONS	Docket No.:	10981801-1

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief under 37 C.F.R. §1.192 is submitted in support of the Notice of Appeal filed June 2, 2005, responding to the final Office Action of March 7, 2005.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Company Deposit Account No. 08-2025.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope, with sufficient postage, addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 20231 on 7-19-05.

Signature: Shana h. East

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is the assignee, Hewlett-Packard Development Company, L.P.

II. RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences that will affect or be affected by a decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 16-30 are pending in the present application. The final Office Action of March 7, 2005, rejected claims 26-30 under 35 U.S.C. §102 as allegedly anticipated by *Worley* (U.S. Patent No. 5,596,733). The final Office Action also rejected claims 16-25 under 35 U.S.C. §103 as allegedly unpatentable over *Roussel* (U.S. Patent No. 6,230,257) in view of *Worley*.

IV. STATUS OF AMENDMENTS

No amendments have been made or requested since the mailing of the final Office Action. A copy of the current claims is attached hereto as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The summary is set forth as an exemplary embodiment of claim 16. Discussions about elements and recitations can be found at least at the cited locations in the specification and drawings.

As embodied in claim 16, an apparatus is provided for performing single-instruction multiple data (SIMD) operations using one multiply-accumulate (MAC) unit. (e.g., paragraph 0005). In this regard, a MAC unit (e.g., reference numeral 41) is coupled to operand buses (e.g., reference numerals 22, 23, and 24) at respective operand inputs (e.g., paragraph 0015, lines 1-8). The MAC unit is configured to latch a first multiple-bit data value during a first cycle and execute the MAC functions on the first multiple-bit data vale during the next subsequent cycle while latching a second multiple-bit data value (e.g., paragraph 0026, lines 2-6, and paragraph 0027, lines 1-3). The MAC unit is further configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus (e.g., reference numeral 47 once the first MAC result is available (e.g., paragraph 30, lines 1-3) and latch a second MAC result responsive to the second multiple-bit data value (e.g., paragraph 0033, lines 1-3). A register (e.g., reference numeral 80) is coupled to the result bus and is configured to latch the first MAC result (e.g., Paragraph 0018, lines 7-12). A miscellaneous logic unit (e.g., reference numeral 32) is coupled between the result bus and the register (e.g., Figure 2), and the miscellaneous logic unit is configured to detect one or more exceptional conditions (e.g., paragraph 0031, lines 1-2, and paragraph 0033, lines 1-3). The miscellaneous logic unit is further configured to generate first and second control signals responsive to at least one certain exceptional condition, wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus (e.g., paragraph 0031, lines 1-8, and paragraph 0033, lines 1-2). When the second control signal is asserted, the first MAC result is driven from the register onto the result bus (e.g., paragraph 0033, lines 3-5). When the second control signal is not asserted, a miscellaneous-unit generated result is driven onto the result bus (e.g., paragraph 0031, lines 1-2, and paragraph 0034, lines 1-3).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 26-30 are rejected under 35 U.S.C. §102 as allegedly anticipated by *Worley* (U.S. Patent No. 5,596,733).

Claims 16-25 are rejected under 35 U.S.C. §103 as allegedly unpatentable over *Roussel* (U.S. Patent No. 6,230,257) in view of *Worley*.

VII. ARGUMENT

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See, *e.g.*, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Further, in order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, *e.g.*, *In Re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981). In addition, "(t)he PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted). Moreover, the Federal Circuit has stated that "(i)t is impermissible, however, to simply engage in hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps." *In re Gorman*, 933 F.2d 982, 987, 18 U.S.P.Q.2d 1885 (1991).

Discussion of 35 U.S.C. §102 Rejections of Claims 26-30

Claim 26 presently stands rejected in the final Office Action under 35 U.S.C. §102 as allegedly anticipated by *Worley* (U.S. Patent No. 5,596,733). Claims 27-30 depend from claim 26, and claim 26 is, therefore, discussed below as an exemplary claim for discussion.

Claim 26 presently reads as follows:

> 26. An apparatus comprising:
> means for producing control signals responsive to a first data value, a second data value, and one or more exceptional conditions, wherein the exceptional conditions result from the execution of a multiply accumulate (MAC) unit over the first and second data values in sequential order, the means for producing configured to detect the one or more exceptional conditions; and
> ***means for arranging a combination selected from a first MAC unit result, a second MAC unit result, and a representation of a specific exceptional condition*** responsive to the plurality of control signals, wherein the control signals direct whether the first MAC unit result and the second MAC unit result should be used or replaced by the representation of the specific exceptional condition, respectively. (Emphasis added).

Applicant respectfully asserts that the cited art fails to disclose at least the features of claim 26 highlighted above. Thus, the 35 U.S.C. §102 rejection of claim 26 is improper.

In this regard, *Worley* describes a multiplexor (MUX) 174 that selects either a value from a functional unit 180 or a value from a storage table 176 depending on whether an exception has been detected for the value being output by the functional unit 180. See Figure 8 and column 10, lines 20-26. Further, in referring to *Worley*, it is asserted in the final Office Action that:

> "For any given instruction, when there is no exception, the Functional Unit A, or Mac unit, supplies a first Mac unit result on the bus, element 178. For another given instruction, when there is no exception, the Functional Unit A, or Mac Unit, supplies a second Mac unit result on the bus, element 178. When there is an exception for either instruction, the storage table, element 176, result {representation of a specific exceptional condition} is driven onto the result bus, element 178)."

Even if it is assumed arguendo that the foregoing Office allegations regarding *Worley* are true, Applicant observes that *Worley* does not discloses a "combination" that is selected from the alleged "first MAC unit result," "second MAC unit result," and "representation of the specific exceptional condition." In particular, the MUX 174 simply selects either a value from the functional unit 180 or a value from the storage table 176, and there is no indication that the selected value is combined with any other value.

The instant application, on the other hand, teaches that results from execution of "first and second data values in sequential order" from the same MAC unit can be associated with the same SIMD instruction, and these results can be combined to form an execution result of the SIMD instruction if there is no exceptional condition detected. Thus, in the absence of an exceptional condition, the "first MAC unit result" and the "second MAC unit result" can be combined. Such combination would not typically occur when the "first MAC unit result" and the "second MAC unit result" are associated with different instructions, as is apparently assumed in the final Office Action. See page 3 of the final Office Action, "**(f)or another given instruction**, when there is no exception..." (emphasis added). Moreover, Applicant respectfully asserts that *Worley* fails to disclose "means for arranging a ***combination*** selected from a first MAC unit result, a second MAC unit result, and a representation of a specific exceptional condition," as described by claim 26. (Emphasis added).

Accordingly, the Office Action fails to establish that the cited art discloses each feature of pending claim 26, and the 35 U.S.C. §102 rejection of claim 26 should, therefore, be overruled.

Discussion of 35 U.S.C. §103 Rejections of Claims 16-19

Claim 16 presently stands rejected in the final Office Action under 35 U.S.C. §103 as allegedly unpatentable over *Roussel* (U.S. Patent No. 6,230,257) in view of *Worley*. Claims 17-19 depend from claim 16, and claim 16 is, therefore, discussed below as an exemplary claim for discussion.

Claim 16 presently reads as follows:

> 16. An apparatus comprising:
> a multiply accumulate (MAC) unit coupled to operand busses at respective operand inputs, the MAC unit configured to latch a first multiple-bit data value during a first cycle and execute the MAC functions on the first multiple-bit data value during the next subsequent cycle while latching a second multiple-bit data value, the MAC unit further configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus once the first MAC result is available and latch a second MAC result responsive to the second multiple-bit data value;
> a register coupled to the result bus and configured to latch the first MAC result; and
> ***a miscellaneous logic unit coupled between the result bus and the register, the miscellaneous logic unit configured to detect one or more exceptional conditions***, the miscellaneous logic unit further configured to generate first and second control signals responsive to at least one certain exceptional condition, wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus, when the second control signal is asserted the first MAC result is driven from the register onto the result bus, and wherein when the second control signal is not asserted a miscellaneous-unit generated result is driven onto the result bus. (Emphasis added).

Applicant respectfully asserts that the combination of *Roussel* and *Worley* fails to suggest at least the features of claim 16 highlighted above. Thus, the 35 U.S.C. §103 rejection of claim 16 is improper.

In this regard, it is candidly admitted in the final Office Action that *Roussel* fails to teach "a miscellaneous logic unit coupled between the result bus and the register, the miscellaneous logic unit configured to detect one or more exceptional conditions." It is, however, alleged that

such features are taught by *Worley*. In particular, it is alleged in the final Office Action that *Worley* teaches:

> "a miscellaneous logic unit coupled between the result bus and the register (Figure 8, elements 174 and 176), the miscellaneous logic unit configured to detect one or more exceptional conditions (column 1, lines 25-57, In order for an exception to be generated, the exception condition must have been detected.)"

However, there is nothing in *Worley* to indicate that logic for detecting the exception condition is coupled "between" the alleged "result bus" and the alleged "register." Indeed, component 174 is a multiplexor, which does not "detect" an exception condition but rather responds to control signals to select between a value from functional unit 180 and a value from the storage table 176. Further, there is nothing to indicate that component 176 "detects" an exception condition either. In this regard, component 176 appears to be a table that simply stores and provides exception values. Moreover, the cited art fails to suggest that logic for detecting an exception condition is coupled between the alleged "result bus" and the alleged "register," and Applicant therefore submits that the cited art fails to suggest "a miscellaneous logic unit coupled between the result bus and the register, the miscellaneous logic unit configured to detect one or more exceptional conditions," as recited by pending claim 16.

For at least the above reasons, Applicant respectfully asserts that the combination of *Roussel* and *Worley* fails to suggest each feature of claim 16, and the 35 U.S.C. §103 rejection of claim 16 should, therefore, be overruled.

In addition to the reasons set forth above, Applicant respectfully asserts that the 35 U.S.C. §103 rejection of claim 16 is improper because the final Office Action fails to allege a suitable grounds for combining *Roussel* and *Worley*. In this regard, for a proper rejection under 35 U.S.C. §103 based on a combination of references, "(t)here must be

some reason, suggest, or motivation found ***in the prior art*** whereby a person of ordinary skill in the field of the invention would make the combination." *In re Oetiker*, 977 F.2d 1443, 1447, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992) (emphasis added). In rejecting claim 16, it is alleged in the Office Action that:

> "(i)t would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Roussel et al. include the claimed miscellaneous logic unit, as taught by Worley, Jr. et al., for the desirable purpose of correcting exceptions that occur during runtime."

However, Applicant submits that the alleged motivation for combining *Roussel* and *Worley* is not found ***in the cited art*** but is instead based on impermissible hindsight reconstruction of Applicant's invention.

In this regard, there is absolutely nothing in *Roussel* to indicate that there is a need for exception conditions to be detected and corrected in the results output by the "execution units," such as the units 130 and 140 depicted in Figure 5. In particular, it is generally well known in the art that systems employing such "execution units" are to be configured to detect and correct for exception conditions. Indeed, even *Worley* admits that detecting and correcting exceptional conditions is well known in the art. See column 2, lines 1-7. *Worley* further describes some drawbacks to several conventional techniques that are sometimes used to correct for exception conditions. See column 2, line 35, through column 4, line 53. However, there is nothing in the cited art to suggest that *Roussel* suffers from any such drawbacks. Moreover, Applicant respectfully submits that the cited art fails to provide a sufficient motivation or reason for using the techniques described by *Worley* to detect and correct exception conditions in the system described by *Roussel*. "Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application

for a showing of the teaching or motivation to combine prior art references." *In re Dembiczcak*, 175 F.3d 994, 50 U.S. P.Q.2d 1614, 1617 (Fed. Cir. 1999).

In addition, even if it is assumed arguendo that it would have been obvious to combine *Roussel* with *Worley*, Applicant observes that, in addition to *Roussel*, only the embodiment depicted by Figure 8 of *Worley* appears to be used in the final Office Action to reject pending claim 16. Moreover, *Worley* describes several other embodiments that, if used in the *Roussel* system, would not suggest all of the claimed features of pending claim 16. Indeed, in several of these other embodiments, a "functional unit" 40 appears to correct for a detected exception condition. See, e.g., column 8, lines 11-15. However, it does not appear that such a "functional unit" is coupled "between" the alleged "result bus" and the alleged "register." Moreover, there is no reason or motivation provided in *Worley* or the cited art as a whole to use the embodiment shown by Figure 8 of *Worley* in lieu of the other embodiments described by *Worley*. Thus, even if it would have been obvious to combine *Roussel* and *Worley* as alleged by the final Office Action, Applicant respectfully asserts that the final Office Action fails to establish a *prima facie* case of obviousness with respect to at least the features of "a miscellaneous logic unit ***coupled between the result bus and the register***," as recited by claim 16. (Emphasis added).

For at least the above reasons, Applicant respectfully asserts that the 35 U.S.C. §103 rejection of claim 16 is improper and should be overruled.

Discussion of 35 U.S.C. §103 Rejections of Claims 20-25

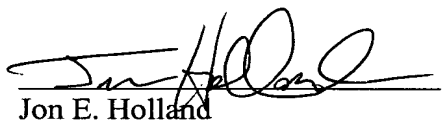
Claims 20-25 presently stand rejected in the final Office Action under 35 U.S.C. §103 as allegedly unpatentable over *Roussel* in view of *Worley*. For at least reasons similar to those described above in the arguments for allowance of claim 16, Applicant respectfully asserts that the combination of *Roussel* and *Worley* is improper. Accordingly, the 35 U.S.C. §103 rejection of claims 20-25 should be overruled.

CONCLUSION

Based on the foregoing discussion, Applicant respectfully requests that the Examiner's final rejections of claims 16-30 be overruled and withdrawn by the Board, and that the application be allowed to issue as a patent with all pending claims.

Respectfully submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: 

Jon E. Holland
Reg. No. 41,077
(256) 704-3900 Ext. 103

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

VIII. CLAIMS - APPENDIX

1-15. Canceled

16. An apparatus comprising:

a multiply accumulate (MAC) unit coupled to operand busses at respective operand inputs, the MAC unit configured to latch a first multiple-bit data value during a first cycle and execute the MAC functions on the first multiple-bit data value during the next subsequent cycle while latching a second multiple-bit data value, the MAC unit further configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus once the first MAC result is available and latch a second MAC result responsive to the second multiple-bit data value;

a register coupled to the result bus and configured to latch the first MAC result; and

a miscellaneous logic unit coupled between the result bus and the register, the miscellaneous logic unit configured to detect one or more exceptional conditions, the miscellaneous logic unit further configured to generate first and second control signals responsive to at least one certain exceptional condition, wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus, when the second control signal is asserted the first MAC result is driven from the register onto the result bus, and wherein when the second control signal is not asserted a miscellaneous-unit generated result is driven onto the result bus.

17. The apparatus of claim 16, wherein the miscellaneous logic unit is configured to identify an exceptional condition responsive to an operand.

18. The apparatus of claim 16, wherein the miscellaneous logic unit is configured to recognize an exceptional condition identified by the MAC unit.

19. The apparatus of claim 18, wherein the miscellaneous logic unit directs the replacement of one of the first and second MAC results with a representation of the exceptional condition.

20. A method for performing single-instruction multiple-data instructions comprising:

applying a plurality of data values on an operand bus for two consecutive cycles;

latching a first data value in a multiply accumulate (MAC) unit during a first cycle;

initiating execution of the multiply and accumulate functions on the first data value and latching a second data value in the MAC unit during a second cycle;

deferring a first MAC unit result responsive to the first data value;

initiating execution of the multiply and accumulate functions on the second data value during a cycle subsequent to the second cycle to generate a second MAC unit result; and

using a miscellaneous logic unit configured to detect one or more exceptional conditions to generate a plurality of control signals responsive to the first data value, the second data value, and an exceptional condition, wherein the control signals direct whether the first MAC unit result and the second MAC unit result should be used or replaced by a representation of a specific exceptional condition, respectively.

21. The method of claim 20, further comprising applying the plurality of control signals to arrange a combination selected from the first MAC unit result, the second MAC unit result, and ~~a~~ the representation of an exceptional condition.

22. The method of claim 20, wherein deferring comprises forwarding the first MAC unit result to a register.

23. The method of claim 20, wherein using a miscellaneous logic unit comprises determining when an operand is invalid.

24. The method of claim 20, wherein using a miscellaneous logic unit comprises determining when an operation in combination with an operand will produce an exceptional condition.

25. The method of claim 20, further comprising forwarding the combination to a result bus.

26. An apparatus comprising:

means for producing control signals responsive to a first data value, a second data value, and ~~an~~ one or more exceptional conditions, wherein the exceptional conditions results from the execution of a multiply accumulate (MAC) unit over the first and second data values in sequential order, the means for producing configured to detect the one or more exceptional conditions; and

means for arranging a combination selected from a first MAC unit result, a second MAC unit result, and a representation of a specific exceptional condition responsive to the plurality of control signals, wherein the control signals direct whether the first MAC unit result and the second MAC unit result should be used or replaced by the representation of the specific exceptional condition, respectively.

27. The apparatus of claim 26, wherein the first MAC unit result is responsive to the first data value.

28. The apparatus of claim 26, wherein the second MAC unit result is responsive to the second data value.

29. The apparatus of claim 26, wherein the exceptional condition is identified by the MAC unit.

30. The apparatus of claim 26, wherein the exceptional condition is identified by the means for producing the plurality of control signals responsive to at least one of the first and second data values and an op code.

IX. EVIDENCE - APPENDIX

None.

X. RELATED PROCEEDINGS - APPENDIX

None.